REMARKS

Claims 1-19 and 24-30 are pending in the present application. By this Response, claim 17 has been amended. Reconsideration and allowance are respectfully requested.

I. Claims 29 and 30

Claims 29 and 30 were added in the Response mailed on March 22, 2004 (hereinafter "Previous Response"). The Office Action mailed on April 19, 2004 states no grounds for rejection of claims 29 and 30.

II. Claim Rejections

Claims 1-5, 7, 9, 11-17, 20-26 and 28 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,119,222 to Shiell et al. Applicants traverse this rejection and respectfully assert that Sheill does not disclose all of the claimed limitations.

As asserted in the Previous Response with regard to claim 1, 14, 24 and 26, Shiell fails to provide for searching a cache system at a first level for an *instruction* and searching the cache system at a second level *for the instruction in parallel* with the first level as claimed. The Examiner has indicated that this argument is not persuasive and contends that "a prefetch of an instruction in a level 2 cache (or higher) can still be executed even though prefetch counters indicate the sought-for contents are most likely in lower cache." Applicants point out, however, that even if a prefetch is executed for an instruction that is already in lower cache, a search for the same instruction in lower cache will not occur in parallel under the teachings of Shiell. Rather, Shiell teaches that the "sought-for" content associated with the prefetch operation represents an instruction that follows fetched content in the program sequence. Indeed, the only way for the same instruction to be simultaneously fetched and prefetched under Shiell would be for a single BTB entry 63i to have identical TARGET and PF ADDR fields, which is clearly contrary to the teachings of the reference.

See, for example Sheill's Abstract, which describes updating "the contents of the prefetch fields (PF0 ADDR; PF1 ADDR) by interrogating *instructions* that are executed *following the associated branching instruction*" (emphasis added). See also Shiell's FIG. 8, which illustrates that prefetching the target of a subsequent instruction "PF0", "PF1" at process 138, whether

unnecessary or not, may be performed simultaneously with fetching the target of the instant (i.e., different) instruction "TARGET" at process 136. Simply put, it is clear from Shiell that an unnecessary prefetch would only occur in parallel with the fetching of a preceding branch instruction. For at least the above reasons, claims 1, 14, 24 and 26 are not anticipated by Shiell. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

Claims 6, 8, 10, 18, 19 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Shiell. Applicants traverse this rejection and assert that Shiell fails to satisfy a prima facie case of obviousness because all of the claimed limitations are not taught or suggested by the reference.

At the outset, Applicants point out that the rejected claims depend from claims 1, 14 and 26, and therefore include the limitations not found in Shiell as already discussed. Furthermore, Shiell teaches away from prefetching content that is already in lower cache (see Col. 13, lines 13-17), as acknowledged by the Examiner. With further regard to claim 10, Applicants assert that Shiell demonstrates no appreciation for front end re-start instructions as claimed. Although it is true that using the claimed parallel searching for front end re-starts substantially improves processing performance, there is no motivation in Shiell to modify the reference to arrive at the claimed approach. Furthermore, with regard to claim 27, Applicants challenge the Examiner's inherency argument and point out that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Without a showing that the claimed shift register and OR gate are necessarily present in the fetch unit 56 of Shiell, Applicants assert that the Examiner's burden of proof has not been met. For at least the above reasons, claims 6, 8, 10, 18, 19 and 27 are patentable over Shiell. Accordingly, Applicants request that the Examiner withdraw the instant rejection.

CONCLUSION

Applicants assert that all claims are in condition for allowance. Applicants respectfully request the Examiner to pass this case to issue at the Examiner's earliest possible convenience.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 703.633.0962.

Respectfully submitted,

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